REMARKS

Claims 1-6, 8-11, 20 and 23-31 are all the claims presently pending in the application. Claims 1-6, 8-11 and 20 have been amended to more particularly define the invention. Claims 23-31 have been added to claim additional features of the invention. Attached hereto is a marked-up version of the changes made to the claims by the current Amendment.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 1-6, 8-11 and 20 stand rejected under the doctrine of obviousness-type double patenting as unpatentable over claims 1-12 of Ito et al. (U. S. Pat. No. 6,426,512). Claims 1-5, 8, 11 and 20 stand rejected under 35 U. S. C. §103(a) are unpatentable over Tanaka et al. (Japan Pat. Pub. No. 9-51139). Claims 6 and 9-10 stand rejected under 35 U. S. C. §103(a) are unpatentable over Tanaka in view of Kimura (U. S. Pat. No. 6,028,877).

These rejections are respectfully traversed in view of the following discussion.

I. APPLICANT'S INVENTION

The claimed invention (as recited, for example, in claim 1) is directed to a semiconductor device including a substrate, an undercoat layer formed on the substrate and including a metal nitride, and a group III nitride compound semiconductor layer formed on the undercoat layer.

Conventional devices include a group III nitride compound semiconductor layer formed on the substrate. However, a lattice mismatch between the substrate and the group III nitride compound semiconductor device causes the group III nitride compound semiconductor device to have a bad crystallinity (Application at page 6, lines 5-19).

The claimed invention, on the other hand, includes a group III nitride compound semiconductor layer which is separated from the substrate by at least the undercoat layer. This feature is important because it helps prevent a lattice mismatch between the substrate and the group III nitride compound semiconductor layer. Therefore, the present invention

provides an inexpensive semiconductor device having a group III nitride compound semiconductor layer with a good crystal structure.

II. THE OBVIOUSNESS-TYPE DOUBLE PATENTING REJECTION

The Examiner alleges that claims 1-6, 8-11 and 20 are not patentably distinct from claims 1-12 of Ito. Applicants submit, however, that the invention encompasses a different subject matter than the claims of Ito and is patentably distinct from the claims of Ito.

First, Applicants would point out to the Examiner that, with respect to this obviousness-type double patenting rejection, the Examiner can rely only on the claims and the subject matter disclosed therein. The Examiner cannot rely upon any part of the specification to support her rejection. Instead, the Examiner must show that each and every feature of the claimed invention is disclosed entirely by the claims on which he relies for the obviousness-type double patenting rejection.

Independent claim 1 of Ito discloses a semiconductor device having a substrate, an undercoat layer containing a metal nitride formed on the substrate, a group III nitride compound semiconductor layer, and a titanium layer interposed between the undercoat layer and the group III nitride compound semiconductor layer. Independent claim 2 of Ito discloses a device similar to the device of claim 1, but the undercoat layer in claim 2 includes a titanium layer and a heat resisting layer (Ito at col. 35, lines 25-32).

However, Applicant submits that claims 1-12 of Ito do not teach or suggest "*a group III nitride compound semiconductor layer formed on said undercoat layer, and separated from said substrate by at least said undercoat layer*" as recited in claim 1, and similarly recited in claim 8. As noted above, conventional devices include a group III nitride compound semiconductor layer formed on the substrate. However, a lattice mismatch between the substrate and the group III nitride compound semiconductor device causes the group III nitride compound semiconductor device to have a bad crystallinity (Application at page 6, lines 5-19).

The claimed semiconductor device, on the other hand, includes a group III nitride compound semiconductor layer which is separated from the substrate by at least an undercoat layer (Application at Figures 1, 9, 11, 12 and 25). The undercoat layer may, therefore, help

prevent a lattice mismatch between the substrate and the group III nitride compound semiconductor layer (Application at page 6, lines 8-12). Therefore, the present invention provides an inexpensive semiconductor device having group III nitride compound semiconductor layer with a good crystal structure (Application at page 4, lines 25-28).

Clearly, these novel features are not taught or suggested by claims 1-12 of Ito. Indeed, claims 1-12 of Ito merely disclose a group III nitride compound semiconductor layer formed on an undercoat layer. Nowhere do claims 1-12 of Ito teach or suggest any other relationship between the substrate, the undercoat and the group III nitride compound semiconductor layer. For example, nowhere do the claims teach or suggest forming the group III nitride compound semiconductor layer on the undercoat layer (e.g., entirely on the undercoat layer).

In the claimed invention, on the other hand, a group III nitride compound semiconductor layer is separated from the substrate by at least an undercoat layer. Nowhere is this feature taught or suggested by any of claims 1-12 of Ito.

Therefore, Applicants submit that claims 1-12 of Ito do not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. THE PRIOR ART REFERENCES

A. The Tanaka Reference

The Examiner alleges that Tanaka makes obvious the invention as recited in claims 1-5, 8, 11 and 20. Applicants submit, however, that there are elements of the claimed invention which are neither taught nor suggested by Tanaka.

Tanaka discloses a semiconductor laser element which includes a substrate 1 and a patterned layer of TiN 2 formed on the substrate 1. A GaN buffer layer 4 is formed on the substrate 1 between the partial TiN layer, and an n-type GaN layer 5 is formed on the buffer layer 4 and the patterned TiN layer 2 (Tanaka at [0012];Figure 1(a)).

However, Applicant submits that Tanaka does not teach or suggest "*a group III nitride compound semiconductor layer formed on said undercoat layer, and separated from said substrate by at least said undercoat layer*", as recited in claim 1, and similarly recited in claim 8. As noted above, unlike conventional semiconductor devices, the claimed

semiconductor device includes a group III nitride compound semiconductor layer which is separated from the substrate by at least an undercoat layer (Application at Figures 1, 9, 11, 12 and 25). The undercoat layer may, therefore, help prevent a lattice mismatch and provide a group III nitride compound semiconductor layer with a good crystal structure (Application at page 4, lines 25-28).

Clearly, these novel features are not taught or suggested by Tanaka. Indeed, Tanaka is directed to a completely different structure than the claimed invention. For example, Tanaka does not even discuss at least one of the objectives (e.g., preventing a lattice mismatch between a group III nitride compound semiconductor layer and a substrate) of the claimed invention.

Specifically, Tanaka teaches a lithographically-patterned TiN layer 2 which includes a "stripe-shaped window [which] is opened at the central part"(Tanaka at [0010]; Abstract) . A GaN buffer layer 4 is then formed on the substrate within this "window" of the patterned TiN layer, an n-type GaN layer 5 is formed on the GaN buffer layer 4, and an N-side electrode is formed on the TiN layer (Tanaka at Figure 1(a)).

This is clearly different from the claimed device in which a group III nitride compound semiconductor layer is separated from the substrate by at least an undercoat layer. Indeed, in Tanaka, at least one group III nitride compound semiconductor layer 4 is formed directly on the substrate, and one layer 5, is formed primarily on the layer 4. Therefore, layer 5 of Tanaka is clearly not separated from the substrate by an undercoat layer.

Further, as noted above, an object of the claimed device is to prevent a lattice mismatch between the substrate and the group III nitride compound semiconductor. Clearly, the patterned TiN layer cannot provide such a function and clearly does not provide the same function as an undercoat layer. Therefore, it is clearly incorrect to equate the TiN layer 2 of Tanaka with the undercoat layer of the claimed invention.

Therefore, Applicant submits that Tanaka clearly does not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

B. The Kimura Reference

The Examiner concedes that Tanaka does not teach or suggest each and every element of the invention as recited in claims 6 and 9-10. However, the Examiner alleges that Kimura makes up for these deficiencies and would have been combined with the Tanaka to form the claimed invention. Applicants submit, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Kimura discloses a gallium nitride based semiconductor laser with an improved aluminum gallium nitride cladding layer between an active region and a substrate (Kimura at Abstract).

However, Applicants submit that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different problems. Specifically, the Tanaka is directed to a laser element with a low threshold value, whereas Kimura is directed to an improved cladding layer. Certainly, no person of ordinary skill in the art would have considered combining these references, absent impermissible hindsight.

Further, the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner merely states that it would have been obvious to combine these references "in order to take advantage of the epitaxial growth arising from the crystal face" which is insufficient to support the combination.

Moreover, Kimura, like Tanaka, does not teach or suggest "*a group III nitride compound semiconductor layer formed on said undercoat layer, and separated from said substrate by at least said undercoat layer*" as recited in claim 1, and similarly recited in claim 8. As noted above, the undercoat layer in the claimed device helps to prevent a lattice mismatch and provide a group III nitride compound semiconductor layer with a good crystal structure (Application at page 4, lines 25-28).

Clearly, Kimura does not teach or suggest these novel features. Indeed, Kimura is directed to a completely different structure than the claimed invention. For example, Kimura does not even discuss at least one of the objectives (e.g., preventing a lattice mismatch between a group III nitride compound semiconductor layer and a substrate) of the

Specifically, as noted above, Kimura is directed to an improved cladding layer. Indeed, the Examiner relies on Kimura as allegedly disclosing a particular substrate.

However, nowhere does Kimura disclose or suggest an undercoat layer, let alone a group III nitride compound semiconductor layer which is separated from a substrate by an undercoat layer. For example, Kimura merely discloses a substrate 501, a buffer layer 102 on the substrate, a GaN contact layer 103 on the buffer layer, an $Al_xGa_{1-x}N$ cladding layer 135 (e.g., $0.01 \leq x < 0.05$) on the contact layer 103, and so on (Kimura at col. 28, lines 14-67).

In other words, Kimura does not even disclose an undercoat layer, let alone a group III nitride compound semiconductor layer formed on the undercoat layer, and separated from the substrate by at least the undercoat layer. Therefore, Kimura clearly does not make up for the deficiencies of Tanaka.

Therefore, Applicants submit that these references would not have been combined and even if combined, there are elements of the claimed invention that are not taught or suggest by the combination. Therefore, the Examiner is respectfully requested to withdraw this rejection.

IV. CONCLUSION

In view of the foregoing, Applicant submits that claims 1-6, 8-11, 20 and 23-31, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

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T36-141808M/KOH

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 4/25/02

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend the claims to read as follows:

1. (Amended) A semiconductor device comprising:

a substrate;

an undercoat layer formed on said substrate and comprising [containing] a metal nitride; and

a group III nitride compound semiconductor layer formed on said undercoat layer, and separated from said substrate by at least said undercoat layer.

2. (Amended) A semiconductor device according to claim 1, wherein said metal nitride directly contacts [a face of said undercoat layer touching] said group III nitride compound semiconductor layer [is formed of said metal nitride].

4. (Amended) A semiconductor device according to claim 1, wherein said undercoat layer comprises [contains] at least one member selected from the group consisting of titanium nitride, zirconium nitride, hafnium nitride, [and] tantalum nitride, and a nitride of a metal alloy.

5. (Amended) A semiconductor device according to claim 1, wherein said substrate comprises [is formed of] one member selected from the group consisting of sapphire, silicon carbide, gallium nitride, silicon, gallium phosphide, and gallium arsenide.

6. (Amended) A semiconductor device according to claim 1, wherein said substrate comprises [is formed from] a cubic crystal material comprising [on] a (111) face on [of] which said undercoat layer is formed.

8. (Amended) A method of forming a semiconductor device, comprising:

forming an undercoat layer on a substrate, said undercoat layer comprising a metal

nitride; and

forming a group III nitride compound semiconductor layer on said undercoat layer, said group III nitride compound semiconductor layer being separated from said substrate by at least said undercoat layer

[A semiconductor device according to claim 1, wherein said undercoat layer is heated at a temperature of from 600 to 1200°C before said group III nitride compound semiconductor layer is formed].

9. (Amended) A method [semiconductor device] according to claim 8 [1], further comprising:

forming a buffer layer of a group III nitride compound semiconductor [interposed] between said group III nitride compound semiconductor layer and said undercoat layer.

10. (Amended) A method [semiconductor device] according to claim 9, wherein said forming said buffer layer comprises forming said buffer layer [is formed] by a metal organic chemical vapor deposition method at a temperature substantially equal to or higher than the temperature for the growth of said group III nitride compound semiconductor layer.

11. (Amended) A method [semiconductor device] according to claim 9, wherein said forming said buffer layer comprises forming said buffer layer [is formed] by any one of a sputtering method, an evaporation method and an ion plating method.

20. (Amended) A semiconductor device according to claim 1, further comprising:

a first electrode provided on said undercoat layer.